MOSTEK

16,384x1-BIT DYNAMIC ROM

MK 28000 P/N

FEATURES

- ☐ 600 ns Maximum Access Time
- ☐ Low Power Dissipation
  Active – 0.02 mW/bit Typ.
  Inactive – .007 mW/bit Typ.
- ☐ EA 4900 and EA 4800 Pin-for-pin Replacement
- ☐ 2K x 8 or 4K x 4 organization with Open Drain Outputs
- ☐ Standard Supplies +5 volts, – 12 volts
- ☐ Ion-Implanted for Full TTL/DTL Compatibility

DESCRIPTION

The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant, P-Channel technology. The MK 28000 is a pin-for-pin replacement for the EA 4900. The MK 28000 may be organized as either a 2K x 8 or 4K x 4 memory.

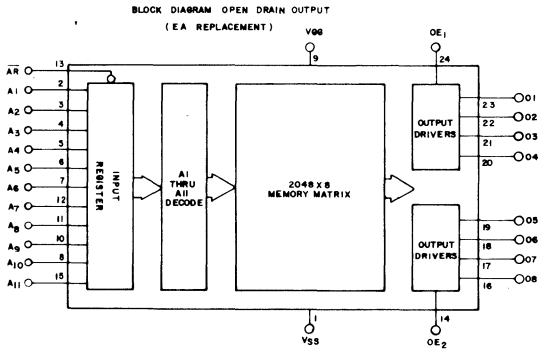
The MK 28000 open drain outputs are divided into two groups with one Output Enable line controlling each group of outputs. This feature allows the MK 28000 to be either a 2K x 8 or a 4K x 4 memory without any internal mask changes. For a 2K x 8 organization, the Output Enables (OE_1, OE_2) are tied together. For a 4K x 4 organization, the four outputs associated with OE_1 are wire-ORed to the four outputs associated with OE_2. OE_1 and OE_2 are inverted with respect to each other and used as the twelfth address input in the 4K x 4 organization.

The internal circuitry of the MK 28000 is dynamic. This features means low standby power consumption when the ROM is not being addressed.

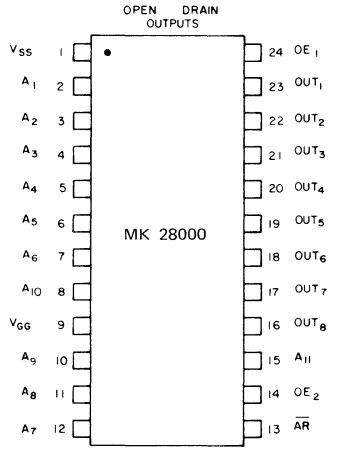
All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

With no address lead time required, system design is simplified; address and $\overline{AR}$ may appear simultaneously.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range (Ambient) ..... 0°C to 70°C
Storage temperature range (Ambient) Ceramic ..... −65°C to +150°C
Storage temperature range (Ambient) Plastic ..... −55°C to +125°C

	PARAMETER	MIN	TYP	MAX	COMMENTS
V_{SS}	Supply Voltage	+4.75V	+5V	+5.25V	
	TTL Reference	–	0	–	
V_{GG}	Supply Voltage	−12.6V	−12V	−11.4V	
V_{IL}	Input Voltage, Logic "0"	V_{GG}		+.8V	
V_{IH}	Input Voltage, Logic "1"	V_{SS} − 1.5V		V_{SS}	Pullup resistors to V_{SS} (≈5K) available as an option

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±5%; V_{DD} = 0V; V_{GG} = −12V ±5%; 0°C ≤ T_A ≤ 70°C)

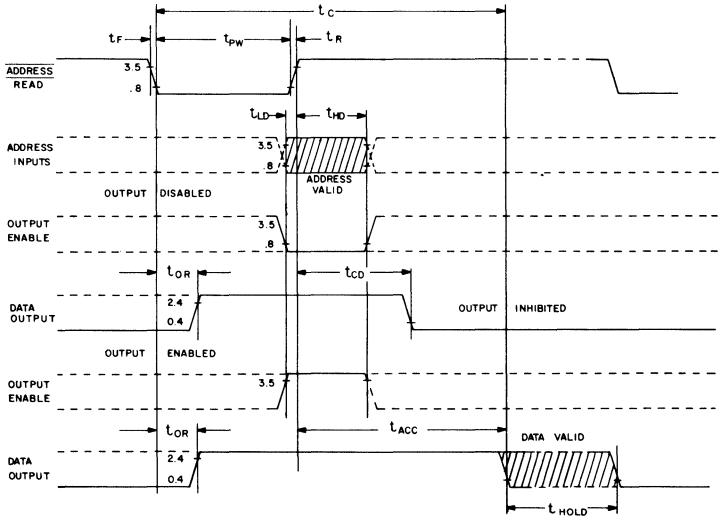
	PARAMETER	MIN	TYP	MAX	COMMENTS
I_{SS}	Supply Current		20 mA	35 mA	See Note 1
I_{GG}	Supply Current		−20 mA	−35 mA	Inputs at V_{SS}
I_{GG}	Supply Current (Standby)		7 mA	12 mA	See Note 1
C_{IN}	Input Capacitance (Address & OE's)		8 pF	10 pF	See Note 2
C_{IN}	Input Capacitance ($\overline{AR}$)		12 pF	15 pF	See Note 2
I_{IN}	Input Leakage			10 µA	See Note 3
R_{IN}	Input Pullup Resistors	3 KΩ		11 KΩ	Optional
V_{OH}	Output Voltage, Logic "1"	2.4V			See Note 4
I_{OL}	Output Leakage Current	−10 µA		+10µA	V_O = V_{SS} −6V, T_A = 25°C (outputs disabled)

	PARAMETER	MIN	TYP	MAX	COMMENTS
t_{PW}	$\overline{AR}$ Precharge Time	400 ns		∞	
t_C	Cycle Time	1 µs + t_R + t_F			t_{ACC} + t_{PW} + t_R + t_F
t_{ACC}	Access Time			600 ns	See note 4
t_{LD}	Address Lead Time	0			
t_{HD}	Address Hold Time	250 ns			
t_R	$\overline{AR}$ Rise Time			100 ns	
t_F	$\overline{AR}$ Fall Time			100 ns	
t_{HOLD}	Data Output Valid Time	2 µs			See note 5
t_{CD}	Output Disable Time			300 ns	See note 4
t_{OR}	Output Reset Time	75 ns		400 ns	See note 4

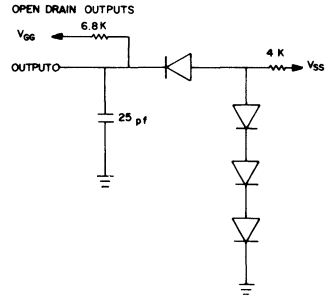
NOTES:

1. Outputs disconnected with no internal pullup resistors.
2. $V_{BIAS} - V_{SS}$ = 0V; f = 1 MHz
3. This parameter is for inputs without pullups (optional)
4. With test circuit shown below
5. or, until the next precharge + T_{OR} [if AR makes a negative transition before t_{HOLD} (min) has elapsed].

TIMING



TEST CIRCUIT



MOSTEK 28000 ROM Punched Card Coding Format[1]

First Card

Cols	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	MOSTEK Part Number[2]
33	Input Pullups (0 = no, 1 = yes, 2 = Selectable Pull-up Option)[5]

Fourth Card

1-9	Data Format[3]
15-28	Logic – ("Positive Logic" or "Negative Logic")
35-57	Verification Code[4]

Data Cards

MOSTEK Format		EA Format
1-4	Decimal Address	
6-13	Output 08-01 (MSB Thru LSB)	
15-17	Octal Equivalent of Output Data	

NOTES:
1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Electronic Arrays Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "EA". Start at column one.
4. Punches as:
   (a) VERIFICATION HOLD – i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS – i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification
   (c) VERIFICATION NOT NEEDED – i.e. the customer will not receive a CVDS and production will begin immediately.
5. Columns 34-47 represent A1–A11, $\overline{AR}$, OE1, OE2 respectively. 0= No pull-up, 1 = Pull-up