SUMMARY OF FLAG OPERATION

Instruction	D7 S	Z		H		P/V	N	D0 C	Comments
ADD A,s; ADC a,s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry
SUB s; SBC A,s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator
AND s	↕	↕	X	1	X	P	0	0	} Logical operations
OR s; XOR s	↕	↕	X	0	X	P	0	0	} Logical operations
INC s	↕	↕	X	↕	X	V	0	•	8-bit increment
DEC s	↕	↕	X	↕	X	V	1	•	8-bit decrement
ADD DD,SS	•	•	X	X	X	•	0	↕	16-bit add
ADC HL,SS	↕	↕	X	X	X	V	0	↕	16-bit add
SBC HL,SS	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry
RLA; RLCA; RRA; RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator
RL s; RLC S; RR s; RRC s; SLA s; SRA s; SRL s	↕	↕	X	0	X	P	0	↕	Rotate and shift locations
RLD; RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator
CPL	•	•	X	1	X	•	1	•	Complement accumulator
SCF	•	•	X	0	X	•	0	1	Set carry
CCF	•	•	X	X	X	•	0	↕	Complement carry
IN r,(C)	↕	↕	X	0	X	P	0	•	Input register indirect
INI; IND; OUTI; OUTD	X	↕	X	X	X	X	1	•	} Block input and output
INIR; INDR; OTIR; OTDR	X	↕	X	X	X	X	1	•	} Z = 0 if B ≠ 0 otherwise Z = 1
LDI; LDD	X	X	X	0	X	↕	0	•	} Block transfer instructions
LDIR; LDDR	X	X	X	0	X	0	0	•	} P/V = 1 if BC ≠ 0 otherwise P/V = 0
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	•	Block search instructions Z = 1 if A = (HL), otherwise Z = 0 P/V = 1 if BC ≠ 0, otherwise P/V = 0
LD A,I; LD A,R	↕	↕	X	0	X	IFF	0	•	The content fo the interrupt enable flip-flop (IFF) is copied into the P/V flag
BIT b,s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag

The following notation is used in this table:

Symbol	Operation
C	Carry/link flag. C=1 if the operation produced a carry from the MSB of the operand or result.
Z	Zero flag. Z=1 if the result of the operation is zero.
S	Sign flag. S=1 if the MSB of the result is one.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V=1 if the result of the operation is even, P/V=0 if the result is odd. If P/V holds overflow, P/V=1 if the result of the operation produced an overflow.
H	Half-carry flag. H=1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N=1 if the previous operation was a subtract. H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care".
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range ⟨0, 255⟩
nn	16-bit value in range ⟨0, 65535⟩

8-BIT LOAD GROUP
'LD'

DESTINATION		SOURCE															
		REGISTER							REG INDIRECT			INDEXED		EXT. ADDR.	IMME.	IMPLIED	
		A	B	C	D	E	H	L	(HL)	(BC)	(DE)	(IX+d)	(IY+d)	(nn)	(n)	I	R
REGISTER	A	7F	78	79	7A	7B	7C	7D	7E	0A	1A	DD 7E d	FD 7E d	3A n n	3E n	ED 57	ED 5F
	B	47	40	41	42	43	44	45	46			DD 46 d	FD 46 d		06 n		
	C	4F	48	49	4A	4B	4C	4D	4E			DD 4E d	FD 4E d		0E n		
	D	57	50	51	52	53	54	55	56			DD 56 d	FD 56 d		16 n		
	E	5F	58	59	5A	5B	5C	5D	5E			DD 5E d	FD 5E d		1E n		
	H	67	60	61	62	63	64	65	66			DD 66 d	FD 66 d		26 n		
	L	6F	68	69	6A	6B	6C	6D	6E			DD 6E d	FD 6E d		2E n		
REG INDIRECT	(HL)	77	70	71	72	73	74	75							36 n		
	(BC)	02															
	(DE)	12															
INDEXED	(IX+d)	DD 77 d	DD 70 d	DD 71 d	DD 72 d	DD 73 d	DD 74 d	DD 75 d							DD 36 d n		
	(IY+d)	FD 77 d	FD 70 d	FD 71 d	FD 72 d	FD 73 d	FD 74 d	FD 75 d							FD 36 d n		
EXT. ADDR.	(nn)	32 n n															
IMPLIED	I	ED 47															
	R	ED 4F															

8-BIT ARITHMETIC AND LOGIC

	REGISTER ADDRESSING							REG. IN-DIR.	INDEXED		IMMED.
	A	B	C	D	E	H	L	(HL)	(IX+d)	(IY+d)	n
'ADD'	87	80	81	82	83	84	85	86	DD 86 d	FD 86 d	C6 n
ADD w CARRY 'ADC'	8F	88	89	8A	8B	8C	8D	8E	DD 8E d	FD 8E d	CE n
SUBTRACT 'SUB'	97	90	91	92	93	94	95	96	DD 96 d	FD 96 d	D6 n
SUB w CARRY 'SBC'	9F	98	99	9A	9B	9C	9D	9E	DD 9E d	FD 9E d	DE n
'AND'	A7	A0	A1	A2	A3	A4	A5	A6	DD A6 d	FD A6 d	E6 n
'XOR'	AF	A8	A9	AA	AB	AC	AD	AE	DD AE d	FD AE d	EE n
'OR'	B7	B0	B1	B2	B3	B4	B5	B6	DD B6 d	FD B6 d	F6 n
COMPARE 'CP'	BF	B8	B9	BA	BB	BC	BD	BE	DD BE d	FD BE d	FE n
INCREMENT 'INC'	3C	04	0C	14	1C	24	2C	34	DD 34 d	FD 34 d	
DECREMENT 'DEC'	3D	05	0D	15	1D	25	2D	35	DD 35 d	FD 35 d	

8-BIT ARITHMETIC AND LOGICAL GROUP

Mnemonic	Symbolic Operation	Flags S	Z		H		P/V	N	C	Op-Code 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A,r	A←A+r	↕	↕	X	↕	X	V	0	↕	10	[000]	r		1	1	4	r
ADD A,n	A←A+n	↕	↕	X	↕	X	V	0	↕	11	[000]	110		2	2	7	000
										←	n	→					001
ADD A,(HL)	A←A+(HL)	↕	↕	X	↕	X	V	0	↕	10	[000]	110		1	2	7	010
ADD A,(IX+d)	A←A+(IX+d)	↕	↕	X	↕	X	V	0	↕	11	011	101	DD	3	5	19	011
										10	[000]	110					100
										←	d	→					101
ADD A,(IY+d)	A←A+(IY+d)	↕	↕	X	↕	X	V	0	↕	11	111	101	FD	3	5	19	111
										10	[000]	110					
										←	d	→					
ADC A,s	A←A+s+CY	↕	↕	X	↕	X	V	0	↕		[001]						s is any of r, n,
SUB A,s	A←A-s	↕	↕	X	↕	X	V	1	↕		[010]						(HL), (IX+d),
SBC A,s	A←A-s-CY	↕	↕	X	↕	X	V	1	↕		[011]						(IY+d) as shown fo
AND s	A←A∧s	↕	↕	X	1	X	P	0	0		[100]						ADD instruction.
OR s	A←A∨s	↕	↕	X	0	X	P	0	0		[110]						The indicated bits
XOR s	A←A⊕s	↕	↕	X	0	X	P	0	0		[101]						replace the [000] in
CP s	A-s	↕	↕	X	↕	X	V	1	↕		[111]						the ADD set above
INC r	r←r+1	↕	↕	X	↕	X	V	0	•	00	r	[100]		1	1	4	
INC (HL)	(HL)←(HL)+1	↕	↕	X	↕	X	V	0	•	00	110	[100]		1	3	11	
INC (IX+d)	(IX+d)←	↕	↕	X	↕	X	V	0	•	11	011	101	DD	3	6	23	
	(IX+d)+1									00	110	[100]					
										←	d	→					
INC (IY+d)	(IY+d)←	↕	↕	X	↕	X	V	0	•	11	111	101	FD	3	6	23	
	(IY+d)+1									00	110	[100]					
										←	d	→					
DEC s	s←s-1	↕	↕	X	↕	X	V	1	•			[101]					s is any of r, (HL), (IX+d), (IY+d) as shown for INC. DEC same format and states as INC. Replace [100] with [101] in OP Code.

Note: The V symbol in the P/V column indicates that the P/V flag contains the overflow of the result of the operation. Similarly the symbol indicates parity. V = 1 means overflow, V = 0 means not overflow, P = 1 means parity of the result is even, P = 0 means parity of the result is odd.

Flag Notation: • = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown.
↕ = flag is affected according to the result of the operation.