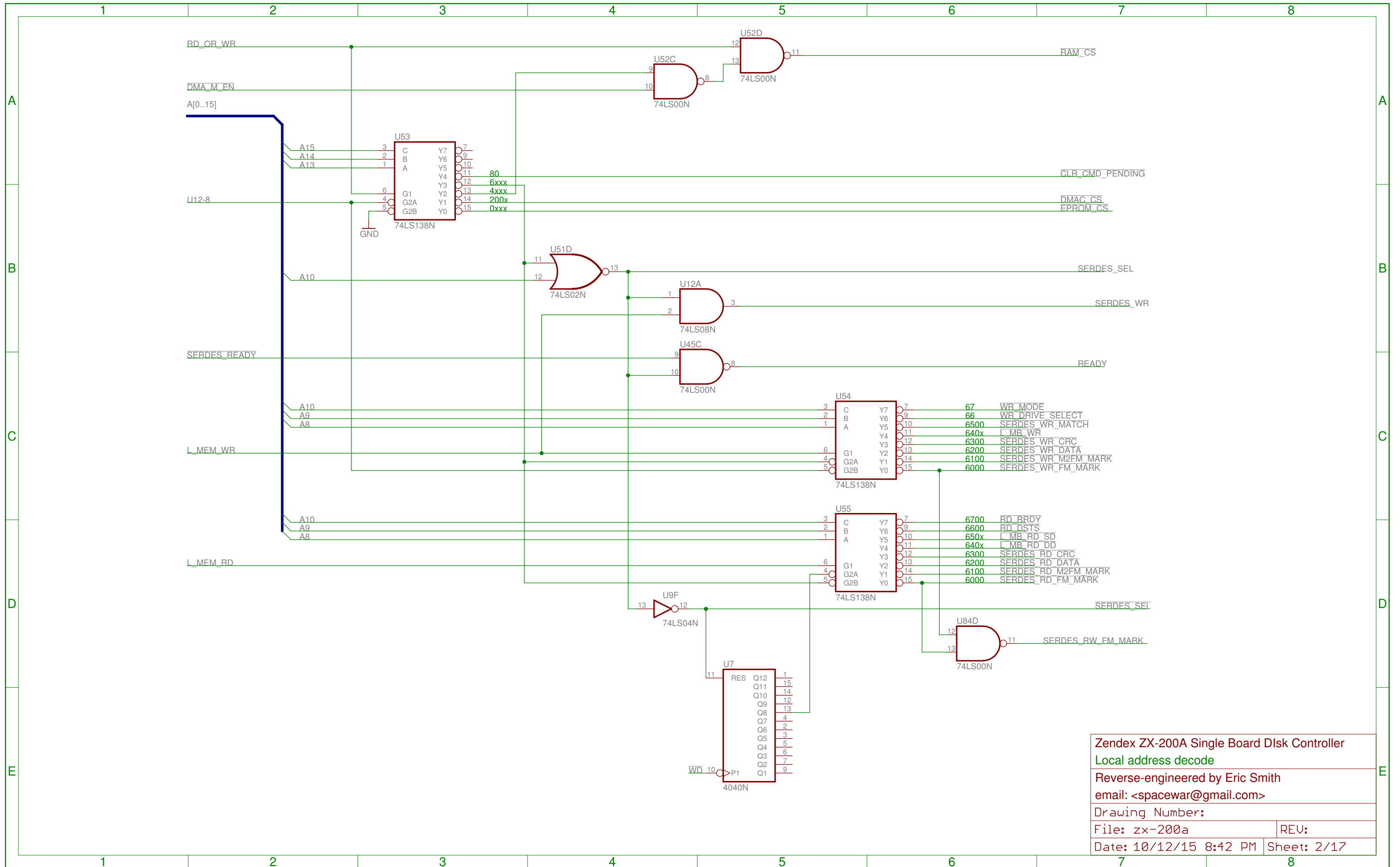
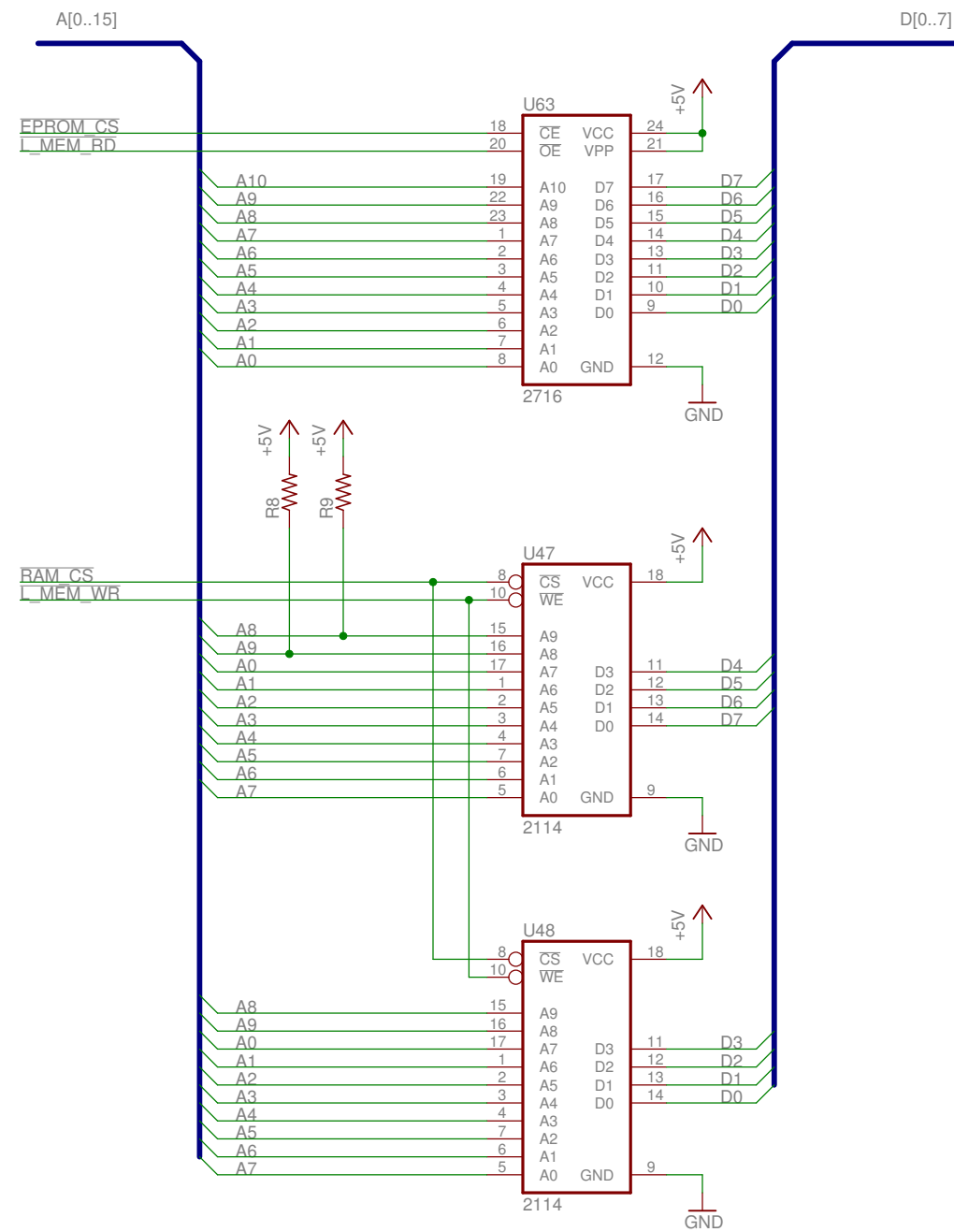


U65 SID input should not be left floating

Zendex ZX-200A Single Board Disk Controller	
Microprocessor	
Reverse-engineered by Eric Smith	
email: <spacewar@gmail.com>	
Drawing Number:	
File: zx-200a	REV:
Date: 10/12/15 8:42 PM	Sheet: 1/17



Zendex ZX-200A Single Board Disk Controller
 Local address decode
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 2/17



Pullup resistors R8 and R9 on address lines A9 and A8, respectively, ensure that DMAC accesses use local memory in the highest 256-byte page of local SRAM, 4300h..43ffh.

Zendex ZX-200A Single Board Disk Controller

Local memory

Reverse-engineered by Eric Smith

email: <spacewar@gmail.com>

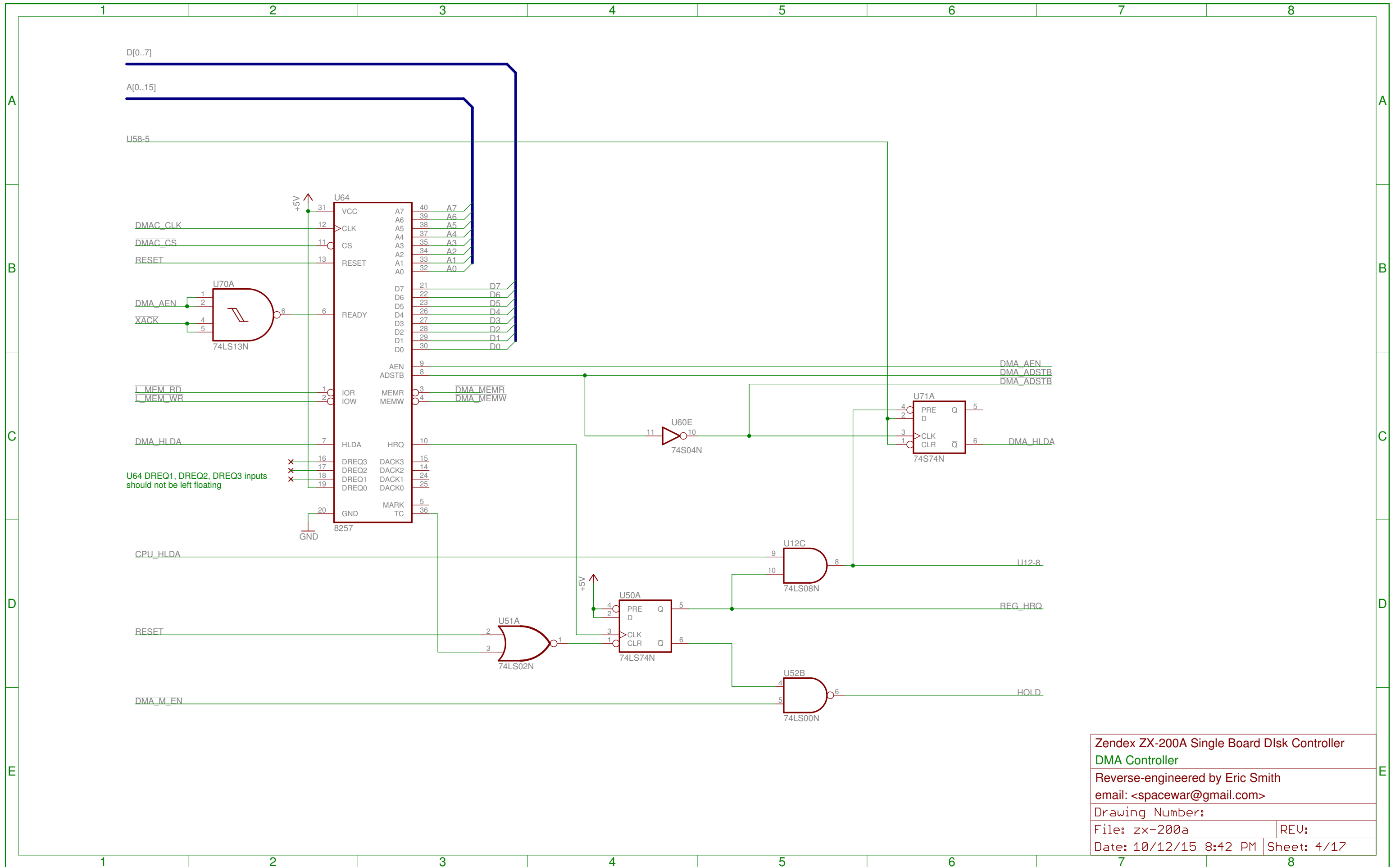
Drawing Number:

File: zx-200a

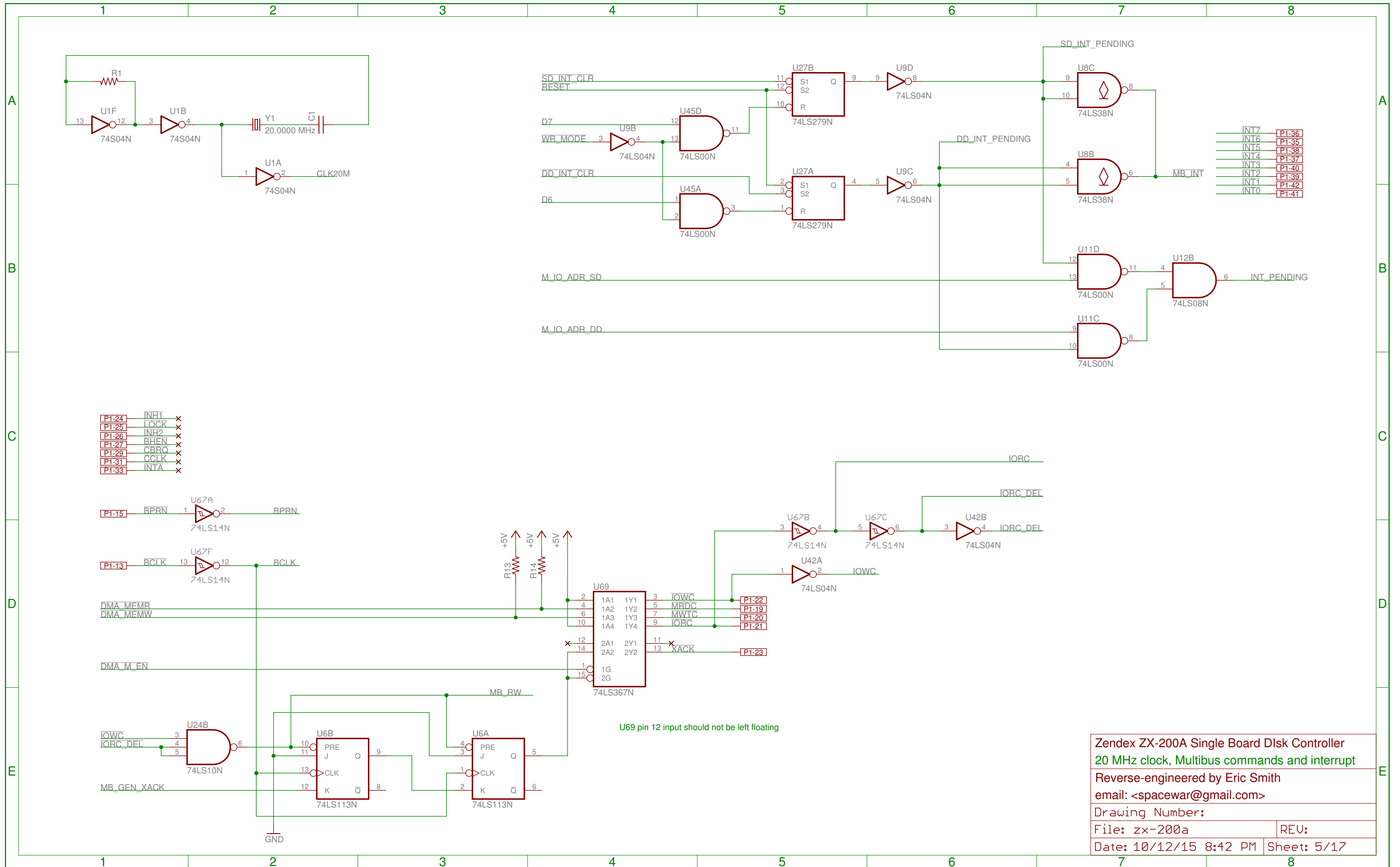
REV:

Date: 10/12/15 8:42 PM

Sheet: 3/17

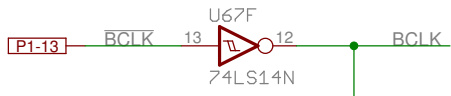
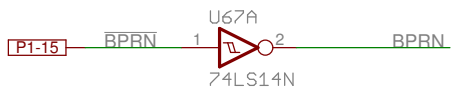


Zendex ZX-200A Single Board Disk Controller
 DMA Controller
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 4/17



P1-24	INH1	x
P1-25	LOCK	x
P1-26	INH2	x
P1-27	BHFN	x
P1-29	CBRO	x
P1-31	CCLK	x
P1-33	INTA	x

INT7	P1-36
INT6	P1-35
INT5	P1-38
INT4	P1-37
INT3	P1-40
INT2	P1-39
INT1	P1-42
INT0	P1-41

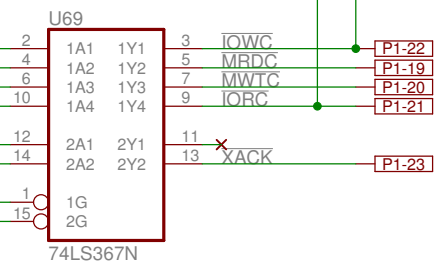
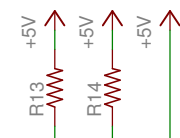


DMA_MEMR
DMA_MEMW

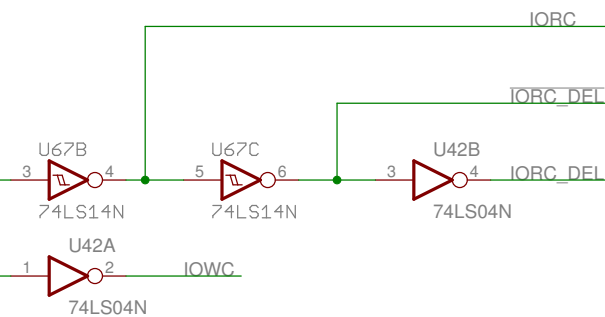
DMA_M_EN

IOWC
IORC_DEI

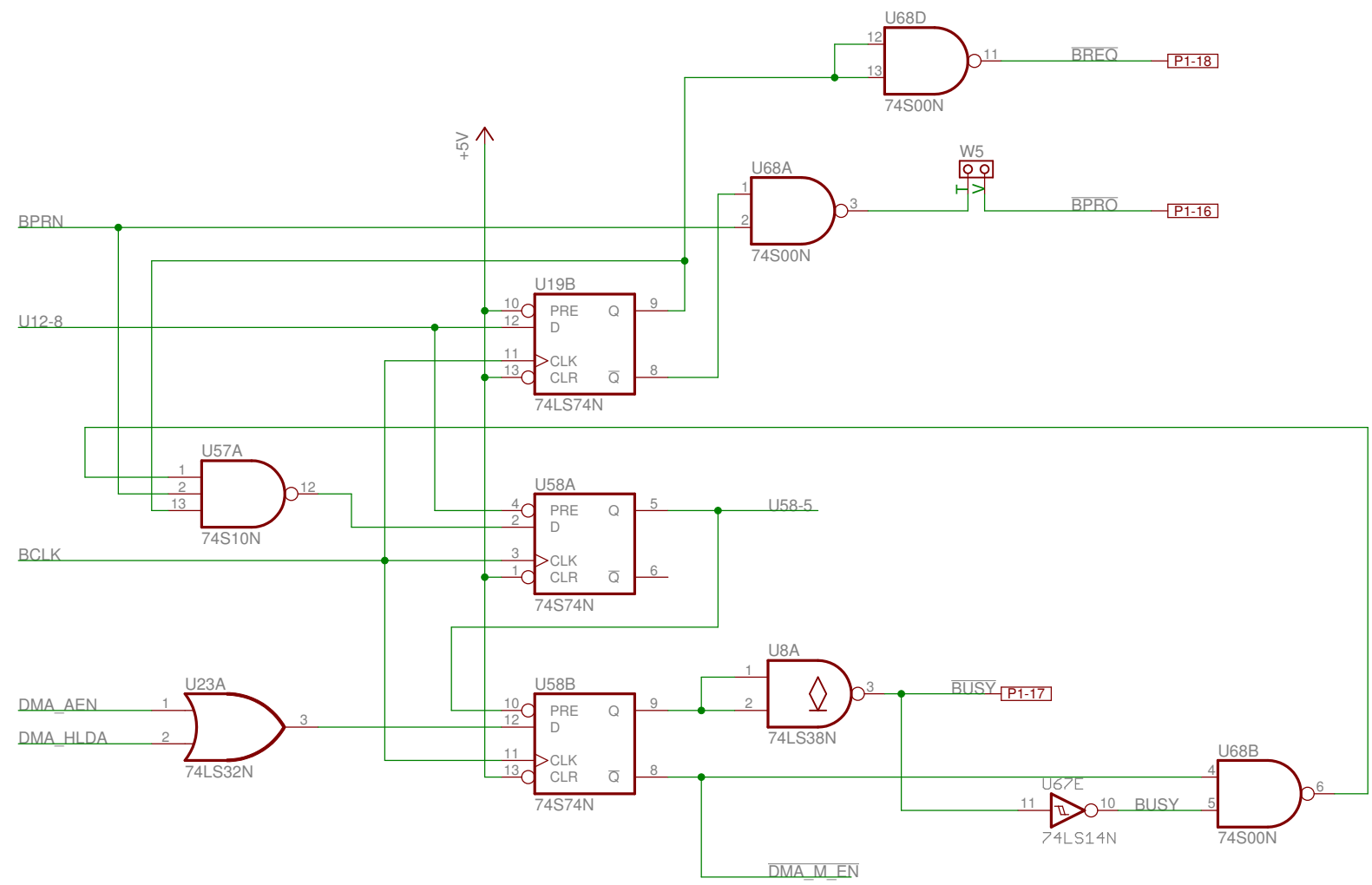
MB_GEN_XACK



U69 pin 12 input should not be left floating



Zendex ZX-200A Single Board Disk Controller	
20 MHz clock, Multibus commands and interrupt	
Reverse-engineered by Eric Smith	
email: <spacewar@gmail.com>	
Drawing Number:	
File: zx-200a	REV:
Date: 10/12/15 8:42 PM	Sheet: 5/17



Zendex ZX-200A Single Board Disk Controller
Multibus arbitration

Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>

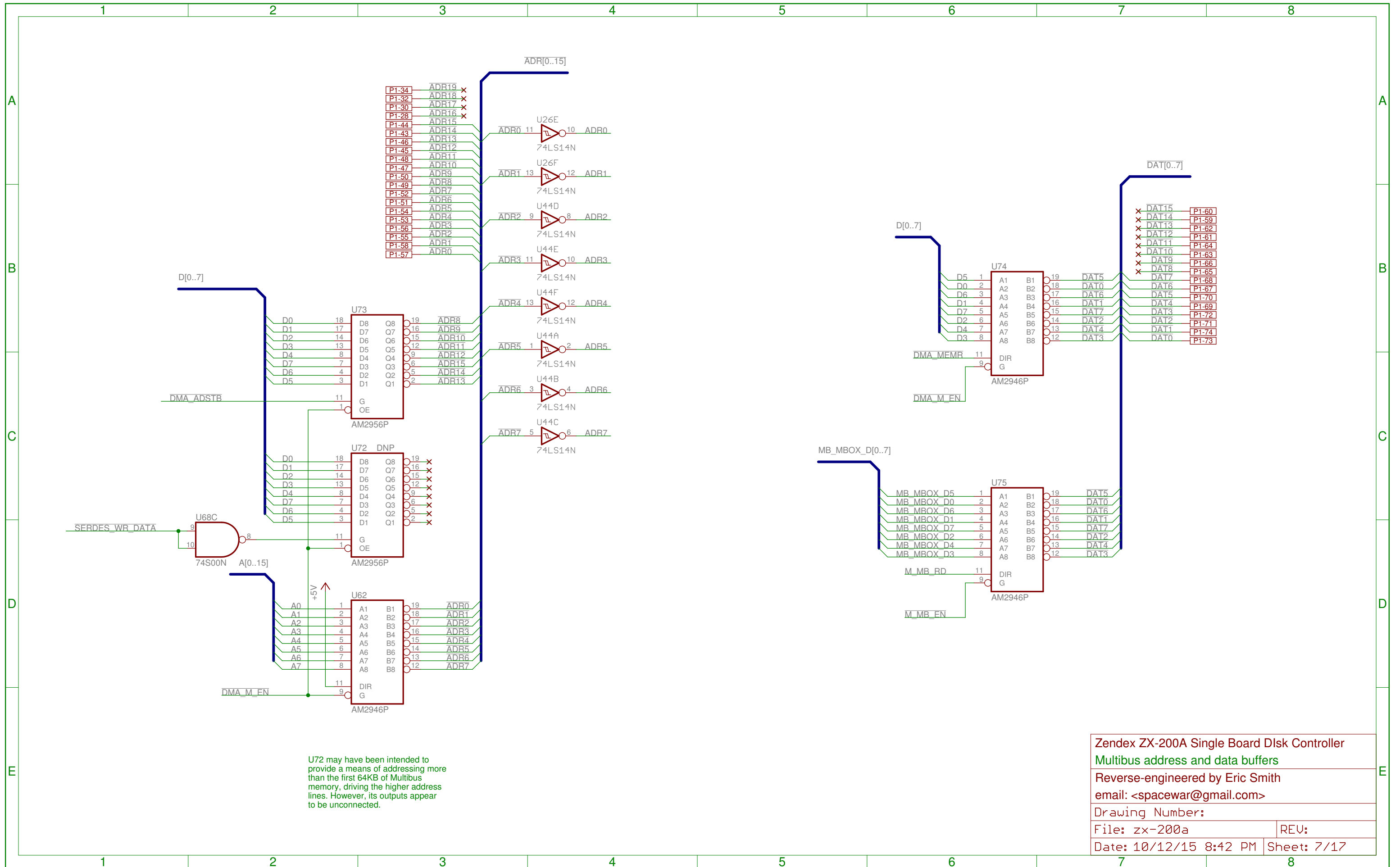
Drawing Number:

File: zx-200a

REV:

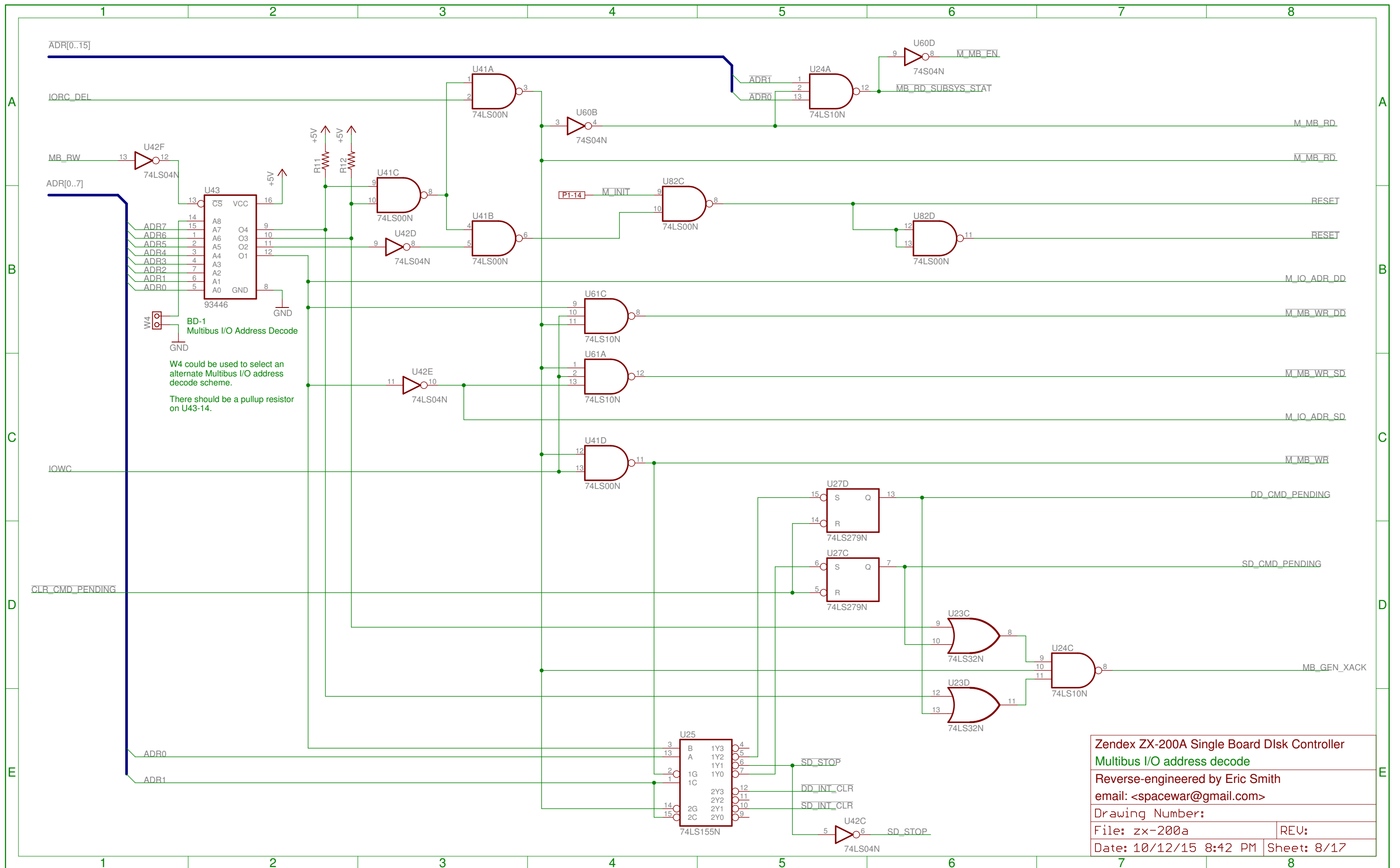
Date: 10/12/15 8:42 PM

Sheet: 6/17



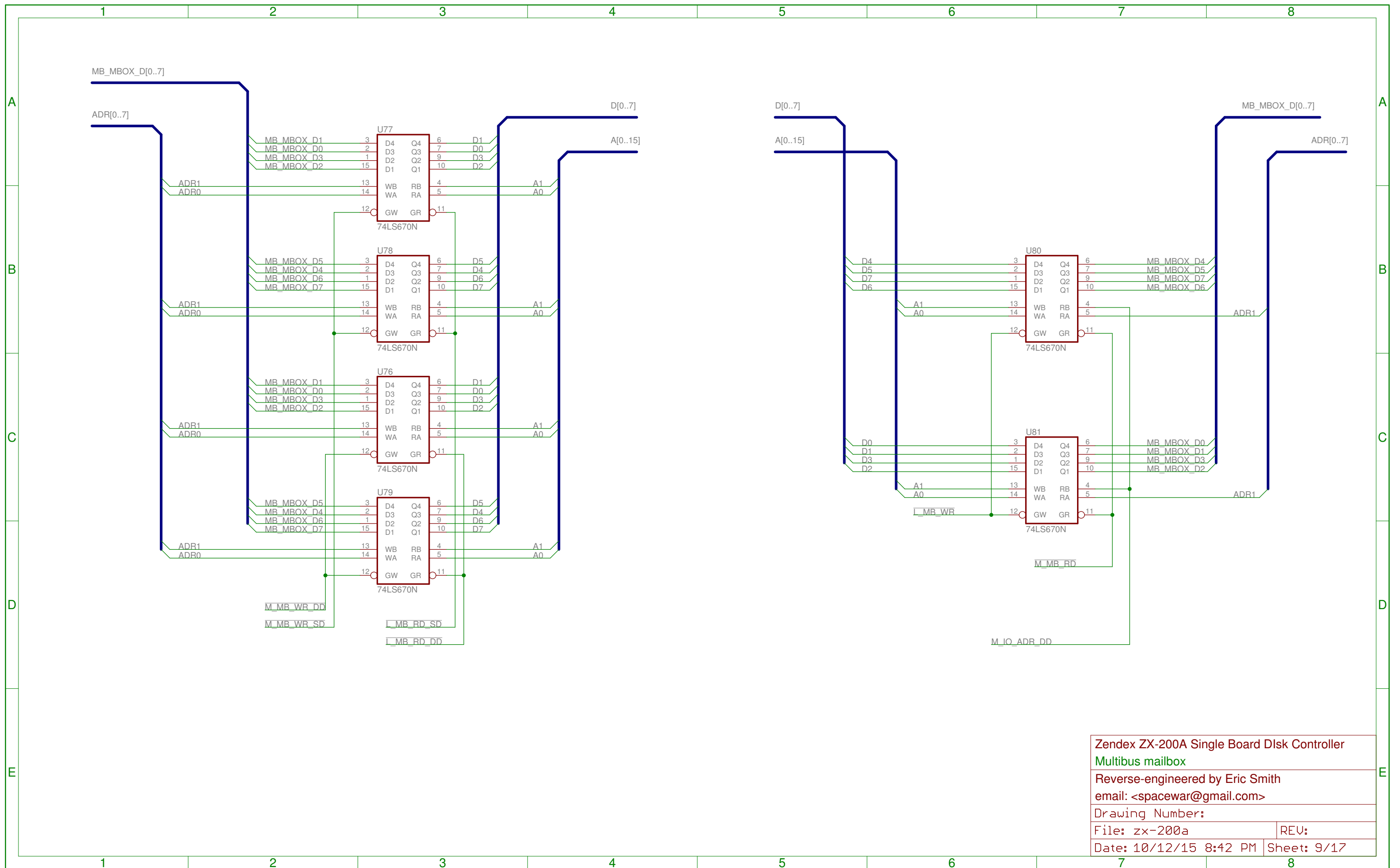
U72 may have been intended to provide a means of addressing more than the first 64KB of Multibus memory, driving the higher address lines. However, its outputs appear to be unconnected.

Zendex ZX-200A Single Board Disk Controller
 Multibus address and data buffers
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 7/17

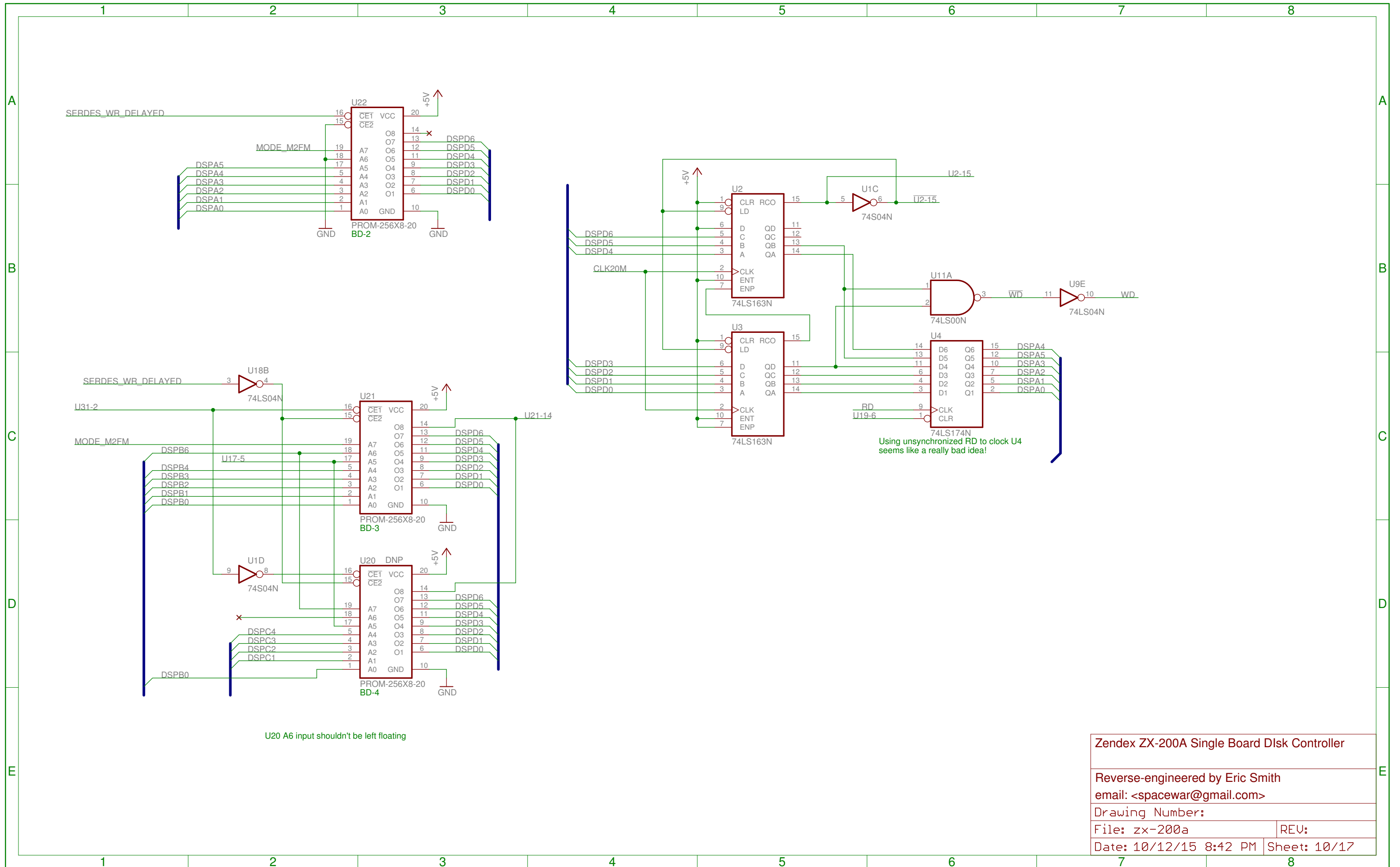


W4 could be used to select an alternate Multibus I/O address decode scheme. There should be a pullup resistor on U43-14.

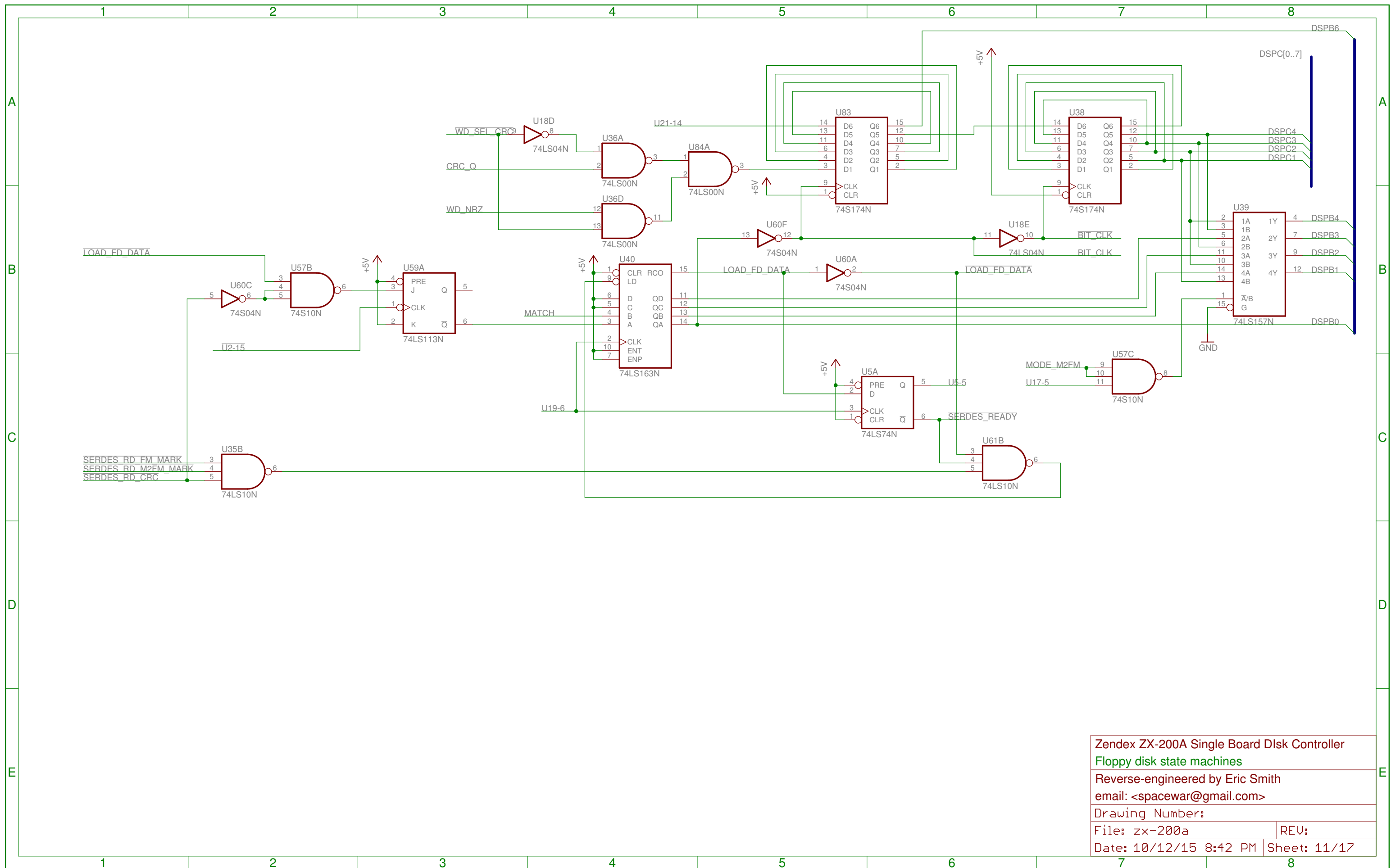
Zendex ZX-200A Single Board Disk Controller
 Multibus I/O address decode
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 8/17



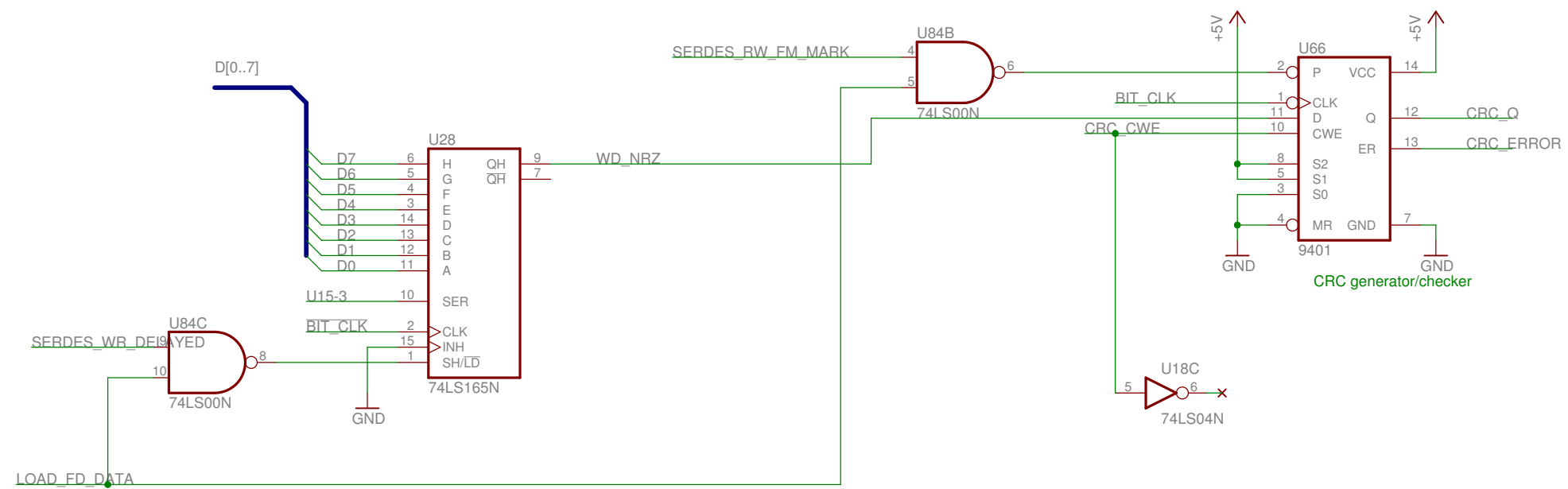
Zendex ZX-200A Single Board Disk Controller
Multibus mailbox
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 9/17



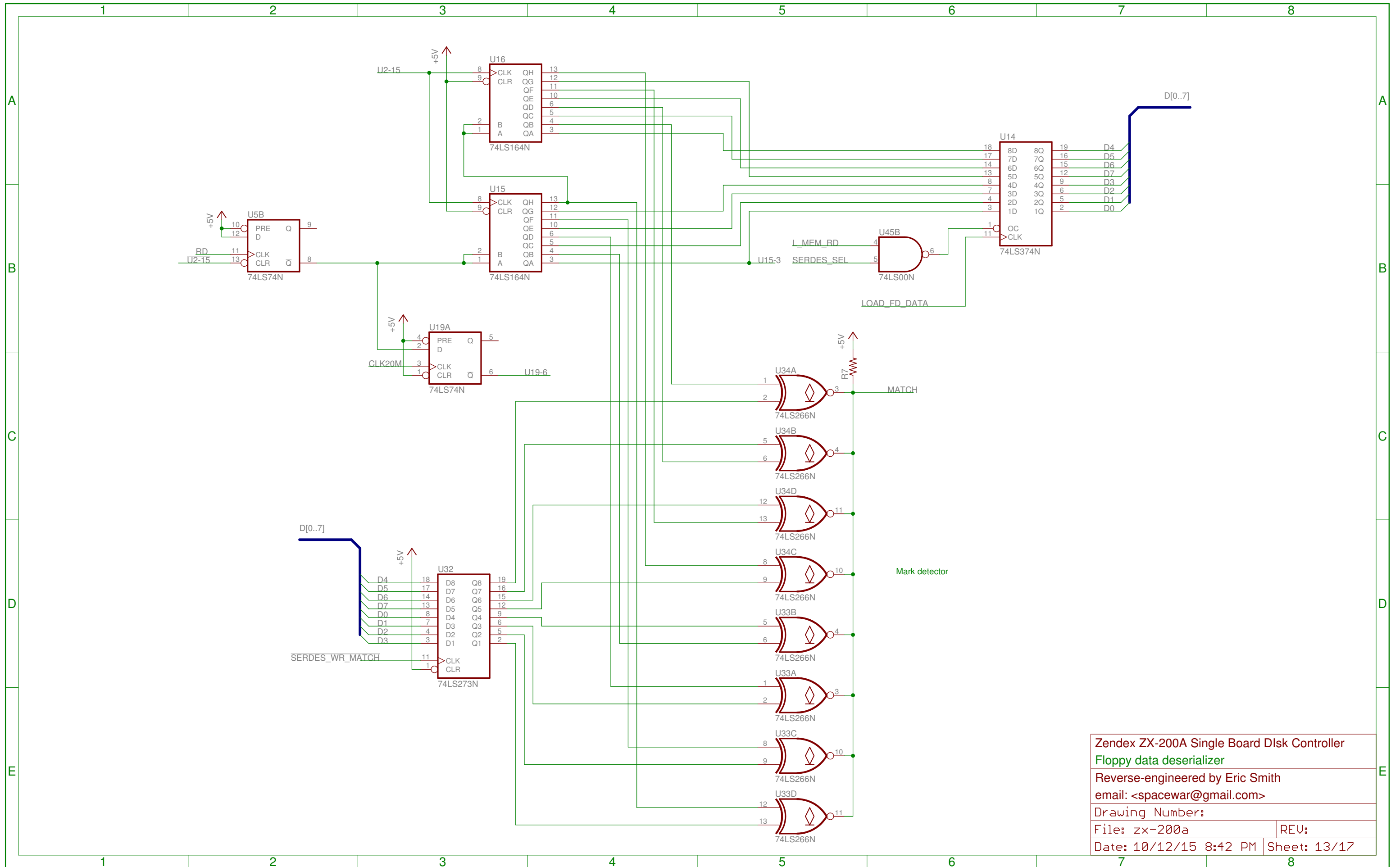
Zendex ZX-200A Single Board Disk Controller
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 10/17



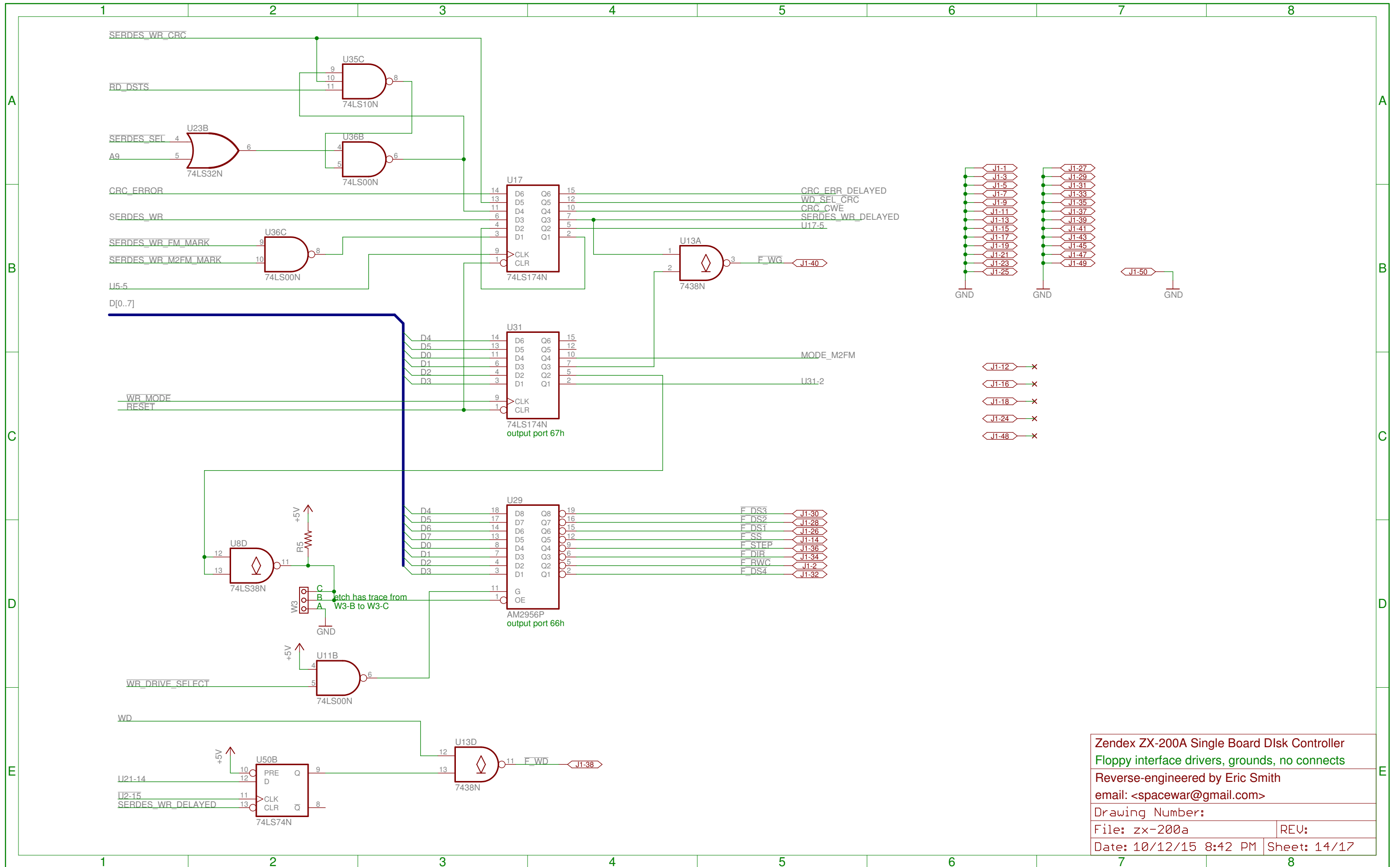
Zendex ZX-200A Single Board Disk Controller
 Floppy disk state machines
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 11/17



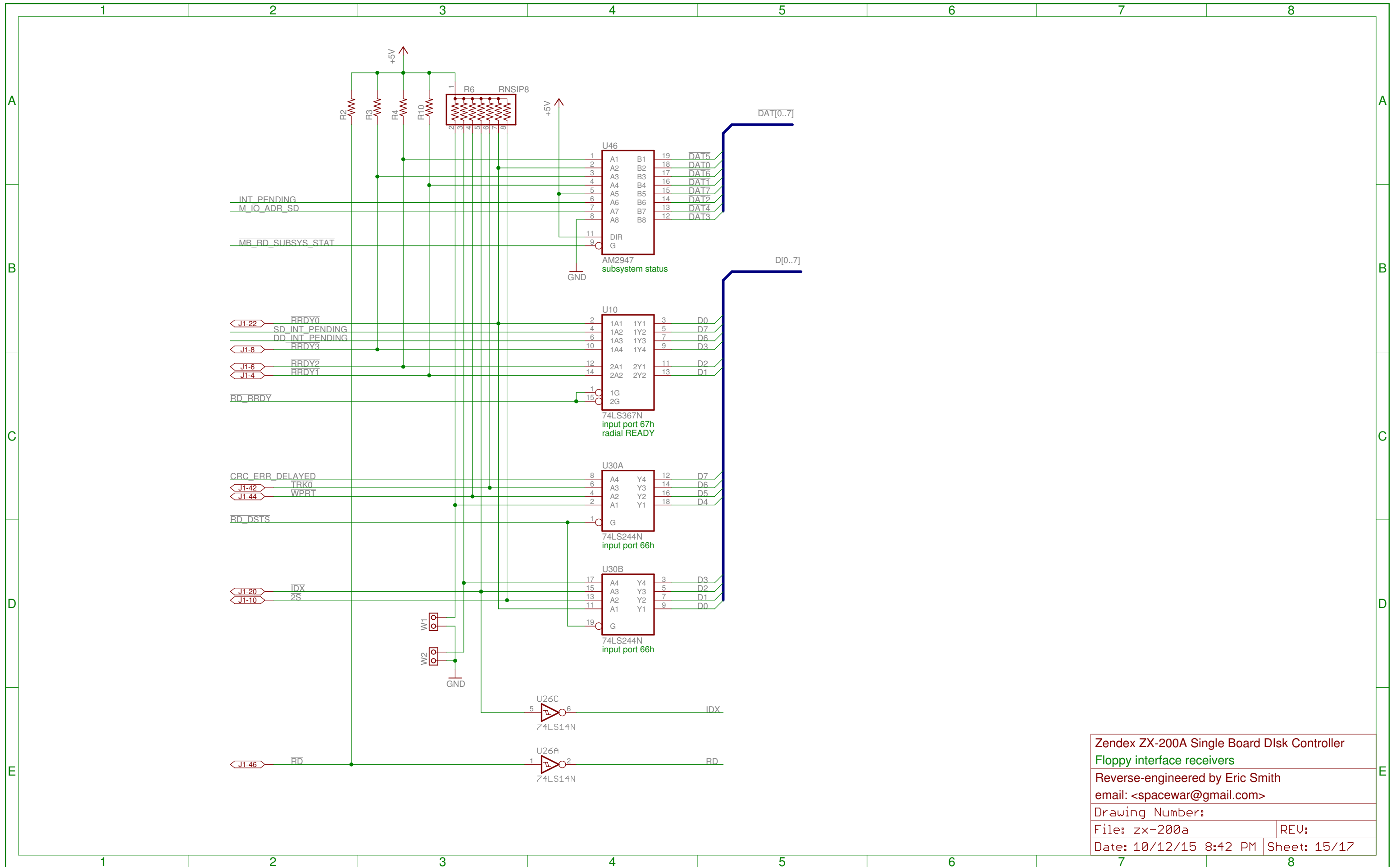
Zendex ZX-200A Single Board Disk Controller
 Floppy data serializer, CRC generator/checker
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 12/17



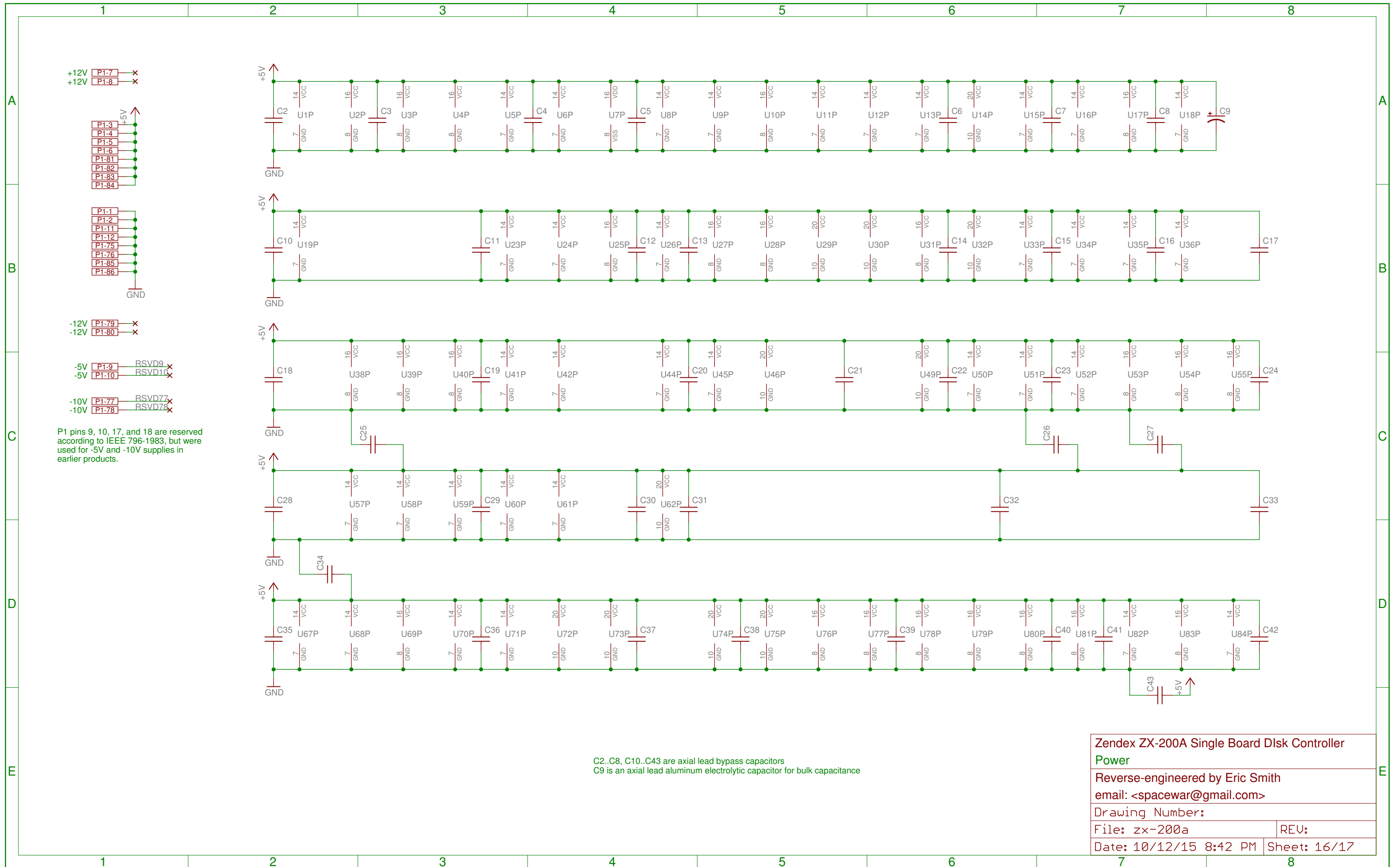
Zendex ZX-200A Single Board Disk Controller
 Floppy data deserializer
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 13/17



Zendex ZX-200A Single Board Disk Controller
 Floppy interface drivers, grounds, no connects
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 14/17



Zendex ZX-200A Single Board Disk Controller
 Floppy interface receivers
 Reverse-engineered by Eric Smith
 email: <spacewar@gmail.com>
 Drawing Number:
 File: zx-200a REV:
 Date: 10/12/15 8:42 PM Sheet: 15/17



+12V P1-7
+12V P1-8

+5V
P1-3
P1-4
P1-5
P1-6
P1-81
P1-82
P1-83
P1-84

P1-1
P1-2
P1-11
P1-12
P1-75
P1-76
P1-85
P1-86

-12V P1-79
-12V P1-80

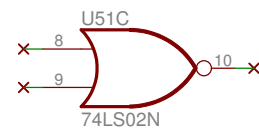
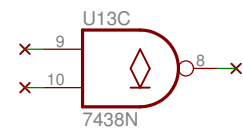
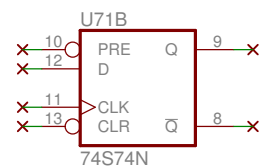
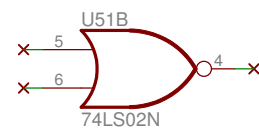
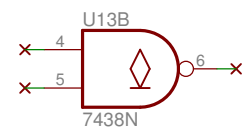
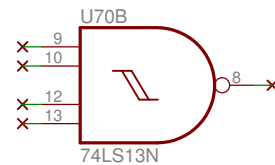
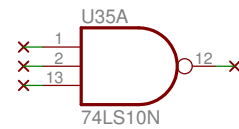
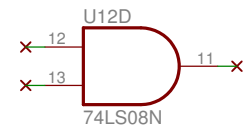
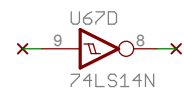
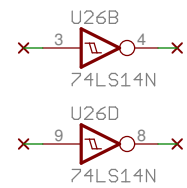
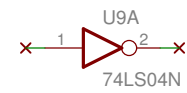
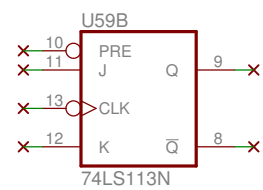
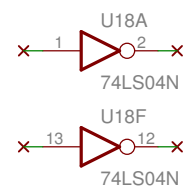
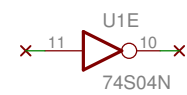
-5V P1-9 RSVD9
-5V P1-10 RSVD10

-10V P1-77 RSVD77
-10V P1-78 RSVD78

P1 pins 9, 10, 17, and 18 are reserved according to IEEE 796-1983, but were used for -5V and -10V supplies in earlier products.

C2..C8, C10..C43 are axial lead bypass capacitors
C9 is an axial lead aluminum electrolytic capacitor for bulk capacitance

Zendex ZX-200A Single Board Disk Controller	
Power	
Reverse-engineered by Eric Smith	
email: <spacewar@gmail.com>	
Drawing Number:	
File: zx-200a	REV:
Date: 10/12/15 8:42 PM	Sheet: 16/17



Need to double-check whether these are really unused.
Unused inputs should not be left floating.

Zendex ZX-200A Single Board Disk Controller	
Unused gates	
Reverse-engineered by Eric Smith	
email: <spacewar@gmail.com>	
Drawing Number:	
File: zx-200a	REV:
Date: 10/12/15 8:42 PM	Sheet: 17/17